

WHAT IS CLAIMED IS:

1. An implantable amplifying circuit for ENG recording of neural signals obtained from nerve electrodes, comprising:
- 5        an input terminal for receiving said signals;  
      an output terminal;  
      nerve protection circuitry connected to said input terminal;  
      a pre-amplifier having an input connected to an output of said nerve protection circuitry;
- 10        an amplifier having an input connected to an output of said pre-amplifier.
2. The implantable amplifying circuit of claim 1 further comprising a DC restoration circuit having an input connected to an output of said amplifier, and having an output connected to said output terminal.
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3. The implantable amplifying circuit of claim 1, further comprising a second input terminal for receiving said signals, wherein said nerve protection circuitry is also connected to said second input terminal.
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4. The implantable amplifying circuit of claim 3, wherein said nerve protection circuitry further comprises a second output, and said pre-amplifier further comprises a second input connected to said second output of said nerve protection circuitry.
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5. The implantable amplifying circuit of claim 4 wherein said nerve protection circuitry comprises:
- 30        a first capacitor in series between said first input terminal and said first input to said pre-amplifier;

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a second capacitor in series between said second input terminal and said second input to said pre-amplifier;

a first resistor connected in shunt configuration between said first input to said pre-amplifier and a connection point;

5 a second resistor connected in shunt configuration between said second input to said pre-amplifier and said connection point; and,

10 a third resistor connected between said connection point and a reference voltage terminal providing a virtual ground terminal in respect of said implantable amplifying circuit.

15 6. The implantable amplifying circuit of claim 1 wherein said nerve protection circuitry comprises a resistor in parallel with one or more capacitors in series, said parallel pair connected between a body ground and a reference voltage terminal providing a virtual ground terminal in respect of said implantable amplifying circuit.

20 7. The implantable amplifying circuit of claim 1 wherein said pre-amplifier comprises:

a low-noise CMOS differential difference input stage having a difference signal output;

a gain stage coupled to receive a difference signal from the difference signal output wherein the difference signal obtained from the input stage is converted to a single-ended signal;

25 a low-power output stage with low output resistance following the gain stage; and

a feedback network connected between the output and input stages.

30 8. The implantable amplifying circuit of claim 1 wherein said amplifier is a band-pass amplifier.

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9. The implantable amplifying circuit of claim 8 wherein said band-pass amplifier comprises a plurality of high-pass filters and a plurality of low-pass negative-feedback amplifiers alternatingly cascaded with said high-pass filters.
10. The implantable amplifying circuit of claim 9 wherein said band-pass amplifier is a programmable-gain band-pass amplifier.
11. The implantable amplifying circuit of claim 10, wherein each low-pass negative-feedback amplifier comprises:
  - a plurality of series-connected resistors forming a resistor string connected between an output terminal and a voltage reference terminal of the low-pass negative-feedback amplifier; and
  - a plurality of selectable switches wherein an end of each selectable switch is connected to an input terminal of the low-pass negative-feedback amplifier and another end of each selectable switch is connected to a nodal point between the resistors in the resistor string.
12. The implantable amplifying circuit of claim 9, wherein each low-pass negative-feedback amplifier comprises an output stage in Darlington configuration operating as class AB amplifier wherein a bias circuit supplying bias to the output stage also carries signal current.
13. The implantable amplifying circuit of claim 1, wherein said programmable-gain band-pass amplifier has a frequency range between approximately 900 Hz and 9 kHz for  $5 \mu V_{\text{peak}}$  input neural signals.

14. The implantable amplifying circuit of claim 1, wherein an equivalent input noise at 3 kHz is lower than  $0.6 \mu V_{rms}$ .
- 5 15. The implantable amplifying circuit of claim 1, having a CMRR higher than 90 dB at 250 Hz.
16. The implantable amplifying circuit of claim 1, having a power consumption lower than 12 mW.
- 10 17. The implantable amplifying circuit of claim 1, wherein said implantable amplifying circuit is powered by an RF telemetry link.
- 15 18. The implantable amplifying circuit of claim 17 having a PSRR higher than 85 dB at 3 kHz.
19. The implantable amplifying circuit of claim 1, wherein said implantable amplifying circuit is powered by a battery.
- 20 20. A pre-amplifier suitable for use in an implantable amplifying circuit, comprising:
- a low-noise CMOS differential difference input stage having a difference signal output;
  - a gain stage coupled to receive a difference signal from the difference signal output wherein the difference signal obtained from the input stage is converted to a single-ended signal;
  - a low-power output stage with low output resistance following the gain stage; and
  - a feedback network connected between the output and input
- 25 30 stages.

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21. The pre-amplifier of claim 20, wherein the low-noise CMOS differential difference input stage comprises two differential pairs comprised of PMOS transistors biased to operate in a weak inversion region.
22. The pre-amplifier of claim 20, wherein the PMOS transistors have a common-centroid crossed-coupled layout.
23. The pre-amplifier of claim 20, wherein the gain stage comprises an amplifier in cascode configuration in which a capacitor, connected between the gates of transistors forming a cascode current mirror circuit and a voltage reference, improves PSRR.
24. The pre-amplifier of claim 20, wherein the low-power output stage with low output resistance comprises an equivalent Darlington pnp transistor.
25. The pre-amplifier of claim 20, wherein the feedback network comprises integrated resistors.
26. An implantable signal carrying circuit comprising:
  - an input for coupling to an implanted electrode;
  - an amplifying circuit comprising a CMOS input stage; and,
  - a protection circuit comprising a high-pass filter coupling the input to the amplifying circuit.
27. The implantable signal carrying circuit of claim 26 wherein the CMOS input stage comprises a pair of CMOS transistors having a common-centroid crossed-coupled layout.

28. A nerve protection circuit suitable for use in an implantable amplifying circuit having a pre-amplifier with high input impedance, comprising a resistor in parallel with one or more capacitors in series, said parallel pair connected between a body ground and a reference voltage terminal providing a virtual ground terminal in respect of said pre-amplifier.
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